#26 7-17-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	**Confirmation No. 3378**
Mitsuaki OSHIMA et al.	:	Docket No. 2000_1420
Serial No. 09/686,467	:	Group Art Unit 2634
Filed October 12, 2000	:	Examiner A. Le
COMMUNICATION SYSTEM	:	

LETTER RE PROPOSED DRAWING AMENDMENTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2634

Sir:

Enclosed herewith is a photocopy of Figs. 2, 10, 17, 29, 48, 65, 67, 93, 112, 131, 138, 144, and 169 marked in red to indicate proposed drawing amendments thereto.

The Examiner is requested to approve such proposed drawing amendments. Formal drawings incorporating such amendments are filed herewith.

Respectfully submitted,

Mitsuaki OSHIMA et al.

By _____
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July 14, 2003

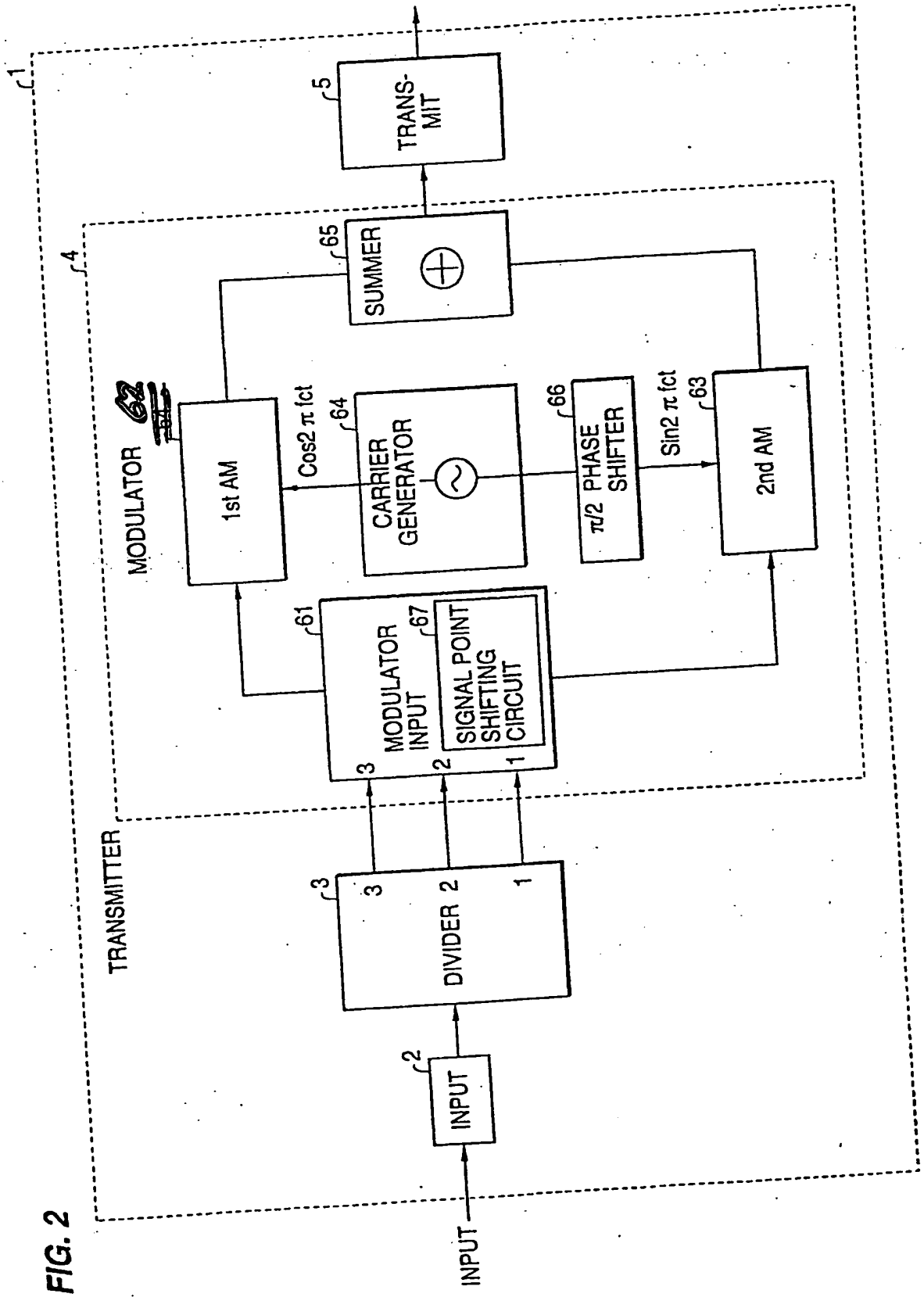
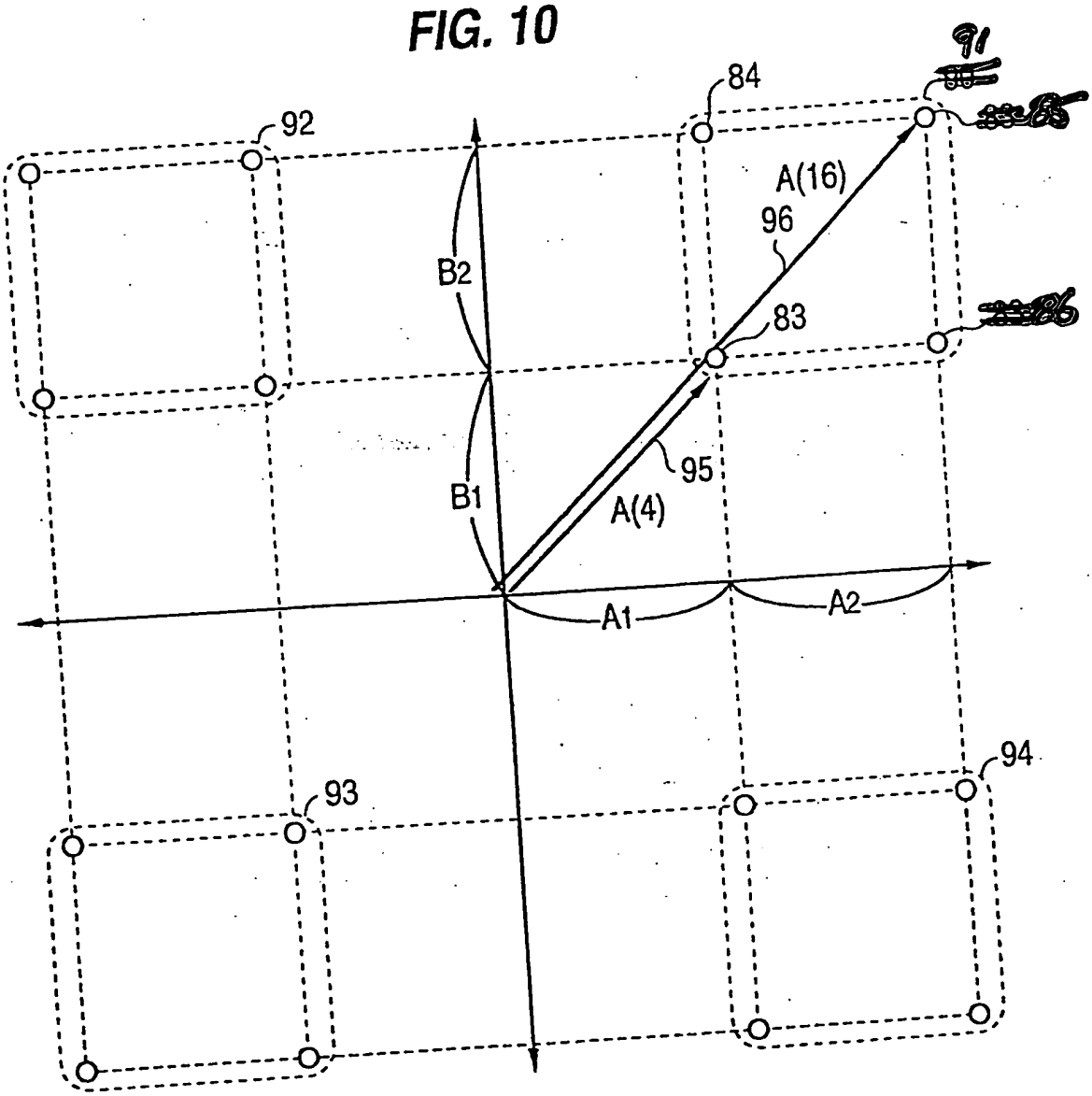

1
TRANSMITTER
2
INPUT
3
DIVIDER 2
4
MODULATOR
5
TRANS-MIT
61
MODULATOR INPUT
62
1st AM
63
2nd AM
64
CARRIER GENERATOR
65
SUMMER
66
π/2 PHASE SHIFTER
67
SIGNAL POINT SHIFTING CIRCUIT
Cos2 π fct
Sin2 π fct
INPUT

FIG. 2

FIG. 10



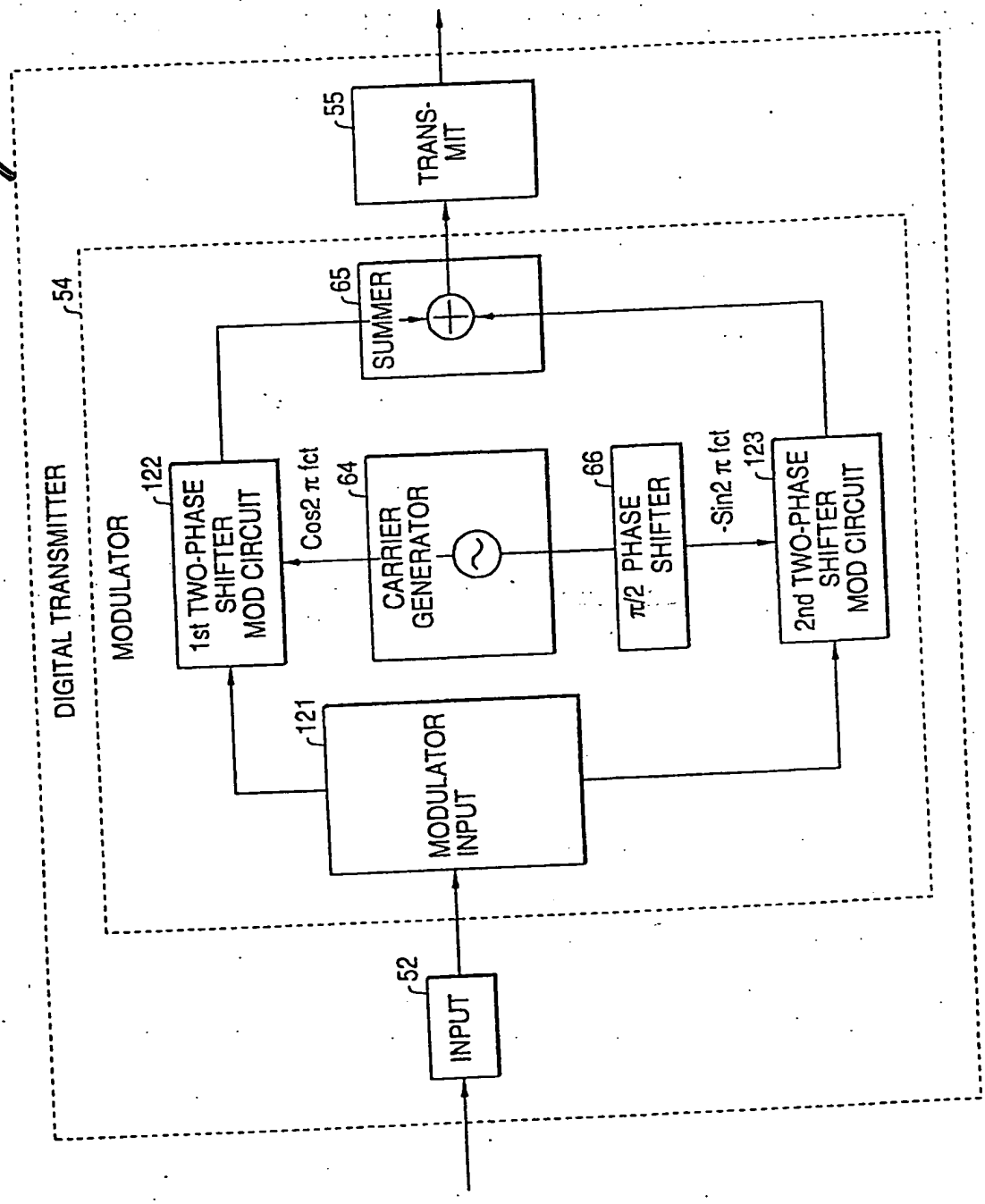

51
DIGITAL TRANSMITTER
54
MODULATOR
55
TRANS-MIT
65
SUMMER
122
1st TWO-PHASE SHIFTER MOD CIRCUIT
Cos2 π fct
64
CARRIER GENERATOR
66
π/2 PHASE SHIFTER
-Sin2 π fct
123
2nd TWO-PHASE SHIFTER MOD CIRCUIT
121
MODULATOR INPUT
52
INPUT

FIG. 17

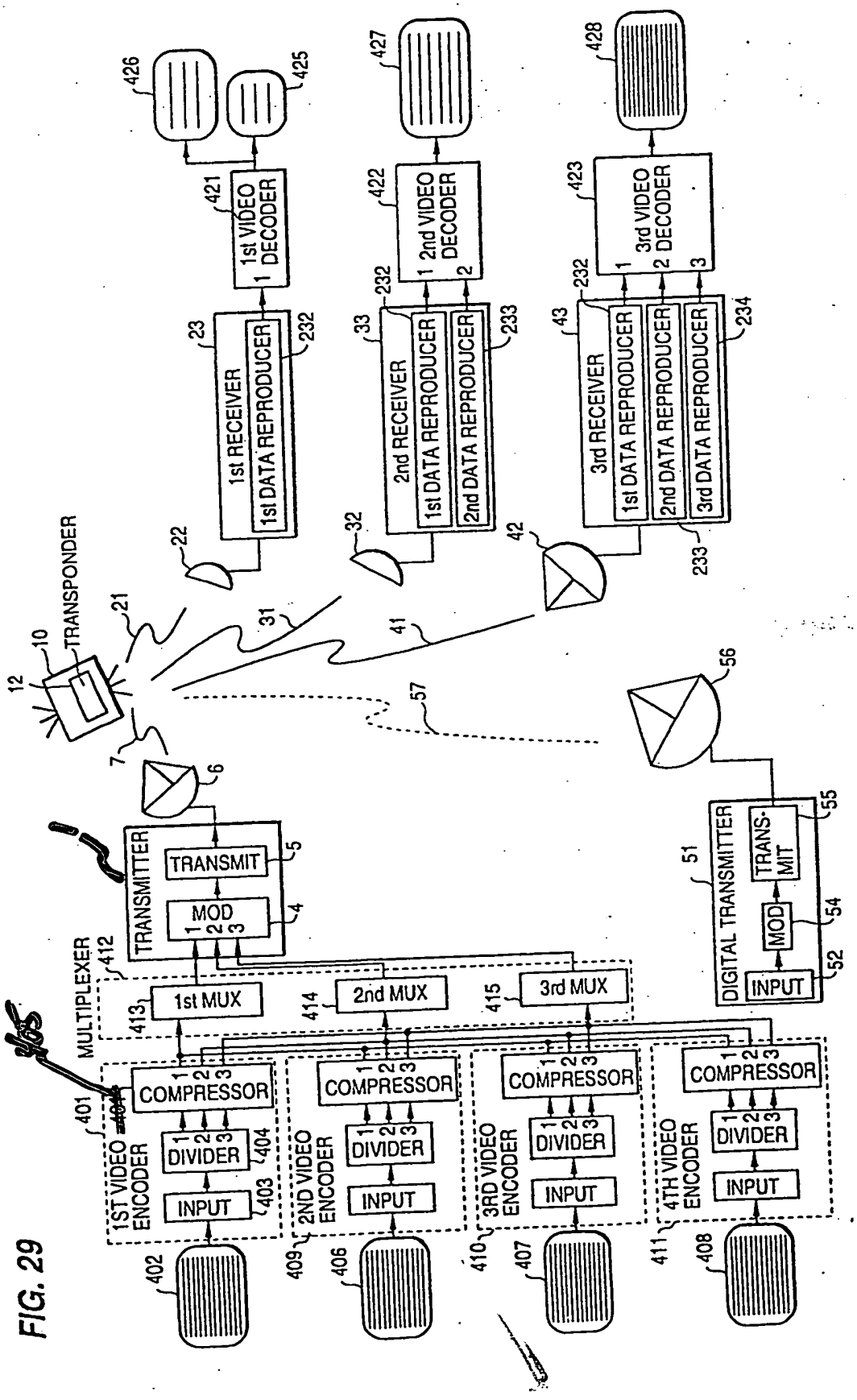

426
425
427
428
421
1st VIDEO DECODER
422
2nd VIDEO DECODER
423
3rd VIDEO DECODER
23
1st RECEIVER
1st DATA REPRODUCER
232
33
2nd RECEIVER
1st DATA REPRODUCER
2nd DATA REPRODUCER
233
43
3rd RECEIVER
1st DATA REPRODUCER
2nd DATA REPRODUCER
3rd DATA REPRODUCER
234
22
32
42
TRANSPONDER
10
12
21
31
41
57
56
7
6
TRANSMITTER
TRANSMIT
MOD
5
4
MULTIPLEXER
412
1st MUX
2nd MUX
3rd MUX
413
414
415
DIGITAL TRANSMITTER
TRANS-MIT
MOD
INPUT
51
55
54
52
COMPRESSOR
DIVIDER
INPUT
401
404
403
1ST VIDEO ENCODER
2ND VIDEO ENCODER
3RD VIDEO ENCODER
4TH VIDEO ENCODER
402
409
406
410
407
411
408

FIG. 29

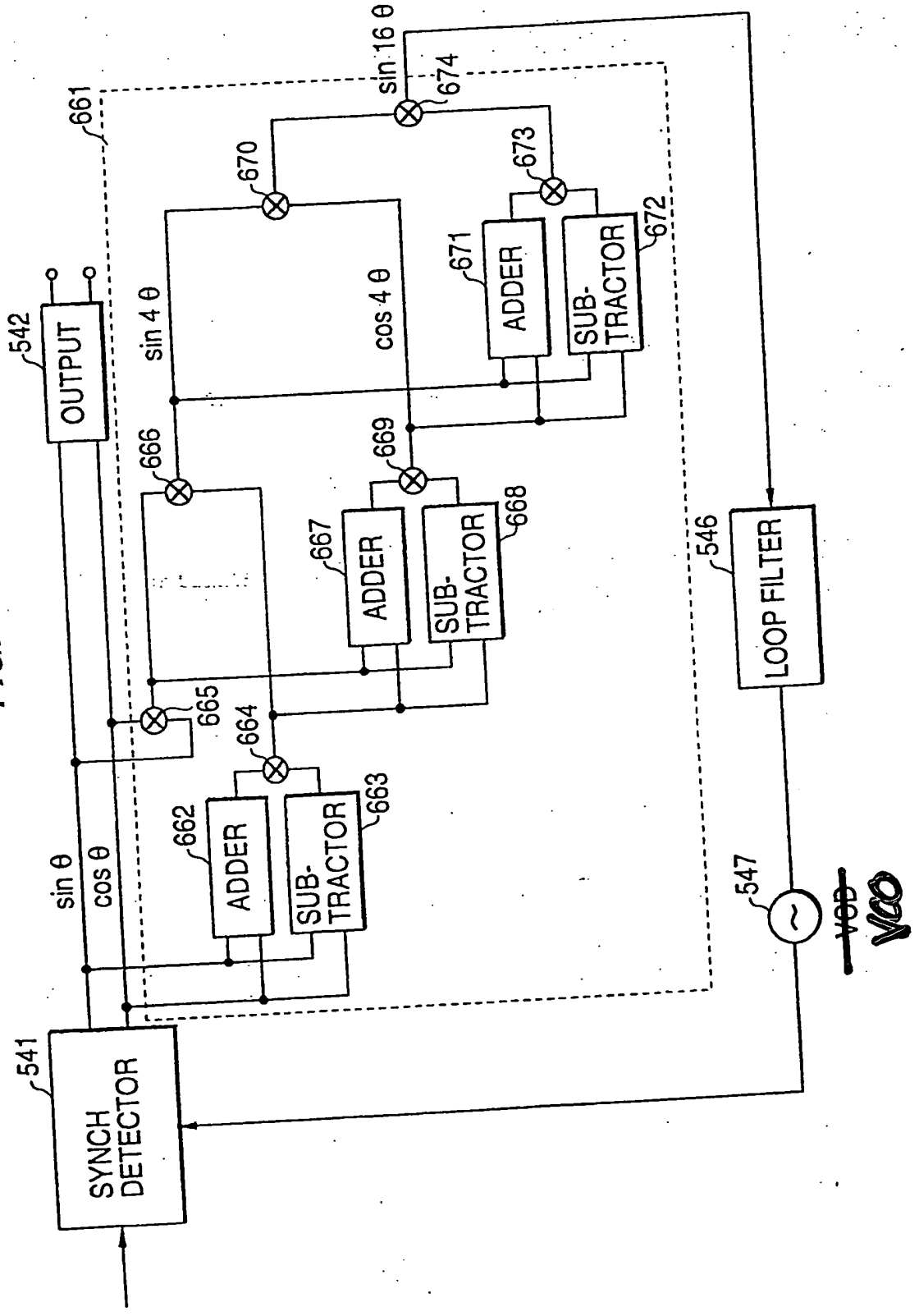
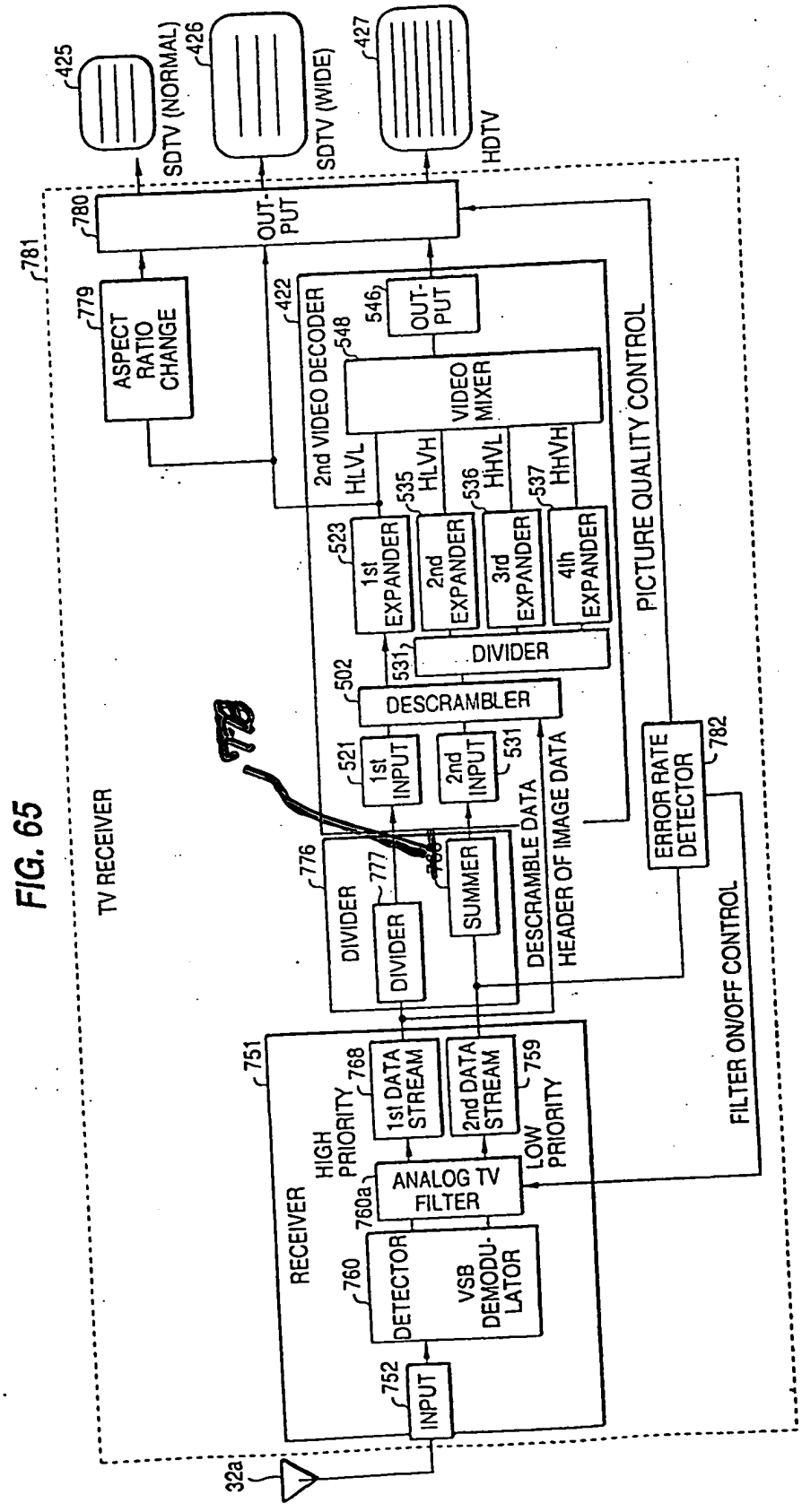

541
SYNCH DETECTOR
542
OUTPUT
661
sin θ
cos θ
662
ADDER
663
SUB-TRACTOR
664
665
666
667
ADDER
668
SUB-TRACTOR
669
sin 4 θ
cos 4 θ
670
671
ADDER
672
SUB-TRACTOR
673
674
sin 16 θ
546
LOOP FILTER
547
VCO
Vco

FIG. 48

FIG. 65


TV RECEIVER
781
425
SDTV (NORMAL)
426
SDTV (WIDE)
427
HDTV
780
OUT-PUT
779
ASPECT RATIO CHANGE
422
2nd VIDEO DECODER
546
OUT-PUT
548
VIDEO MIXER
HLVL
535 HLVH
536 HHVL
537 HHVH
523
1st EXPANDER
2nd EXPANDER
3rd EXPANDER
4th EXPANDER
531
DIVIDER
502
DESCRAMBLER
521
1st INPUT
2nd INPUT
531
DESCRAMBLE DATA
HEADER OF IMAGE DATA
PICTURE QUALITY CONTROL
782
ERROR RATE DETECTOR
776
DIVIDER
777
DIVIDER
SUMMER
FILTER ON/OFF CONTROL
751
RECEIVER
HIGH PRIORITY
768
1st DATA STREAM
2nd DATA STREAM
759
LOW PRIORITY
ANALOG TV FILTER
760a
760
DETECTOR
VSB DEMODU-LATOR
752
INPUT
32a

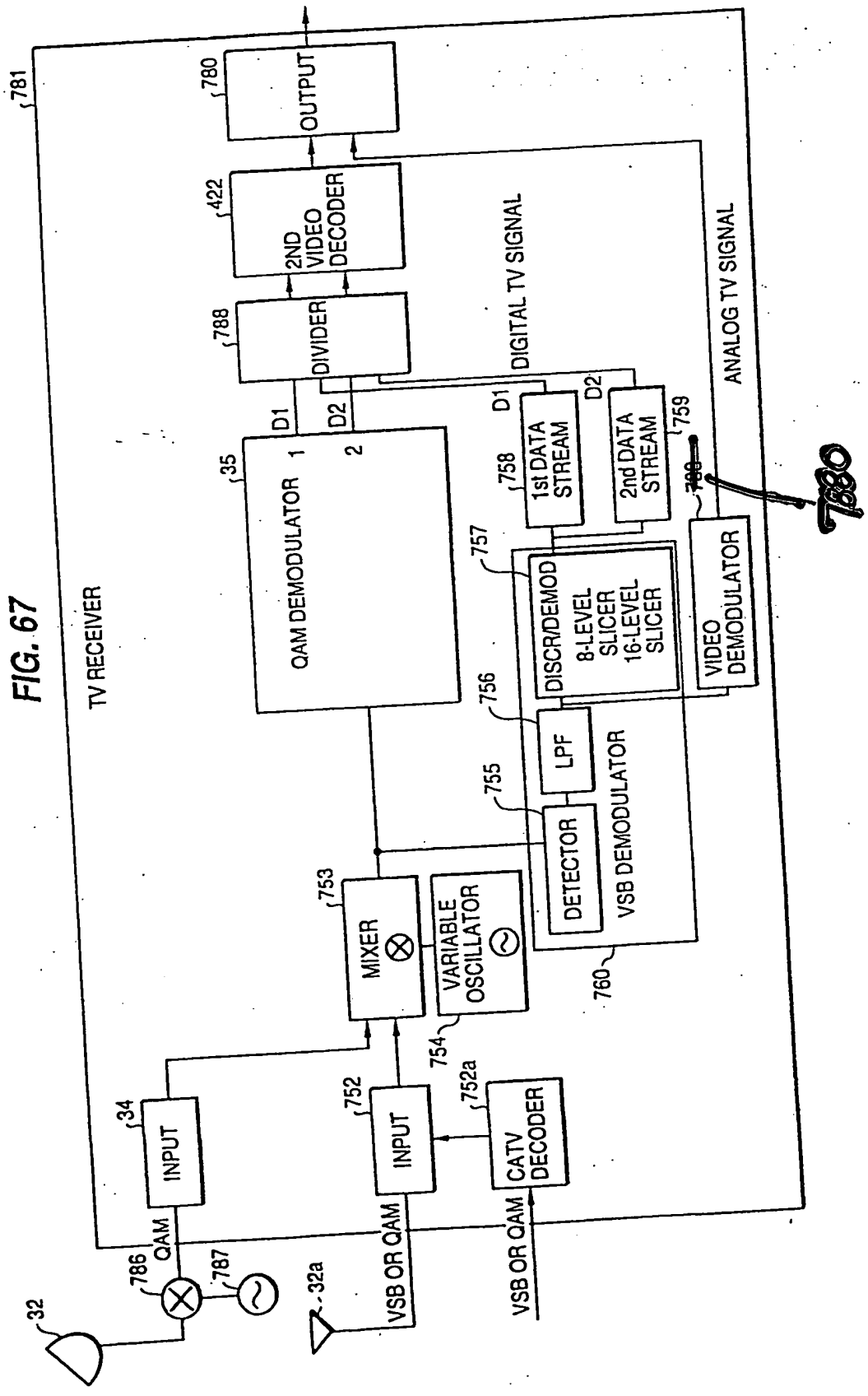

TV RECEIVER
781
780
OUTPUT
422
2ND VIDEO DECODER
788
DIVIDER
DIGITAL TV SIGNAL
ANALOG TV SIGNAL
D1
D2
35
QAM DEMODULATOR
1
2
758
1st DATA STREAM
759
2nd DATA STREAM
760
757
DISCR/DEMOD
8-LEVEL SLICER
16-LEVEL SLICER
VIDEO DEMODULATOR
756
LPF
755
DETECTOR
VSB DEMODULATOR
753
MIXER
VARIABLE OSCILLATOR
754
752
INPUT
752a
CATV DECODER
34
INPUT
786
QAM
787
32
32a
VSB OR QAM
VSB OR QAM

FIG. 67

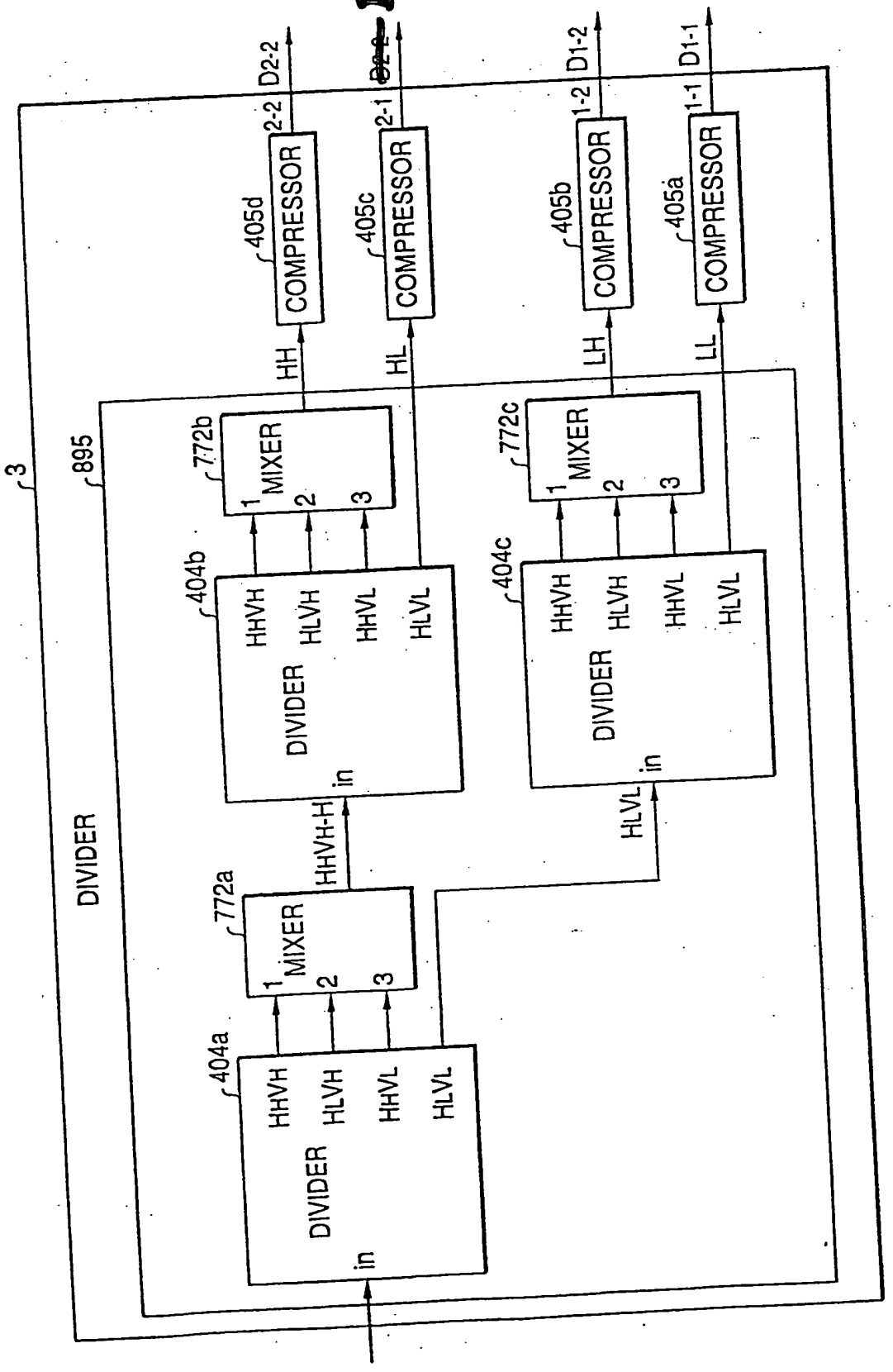
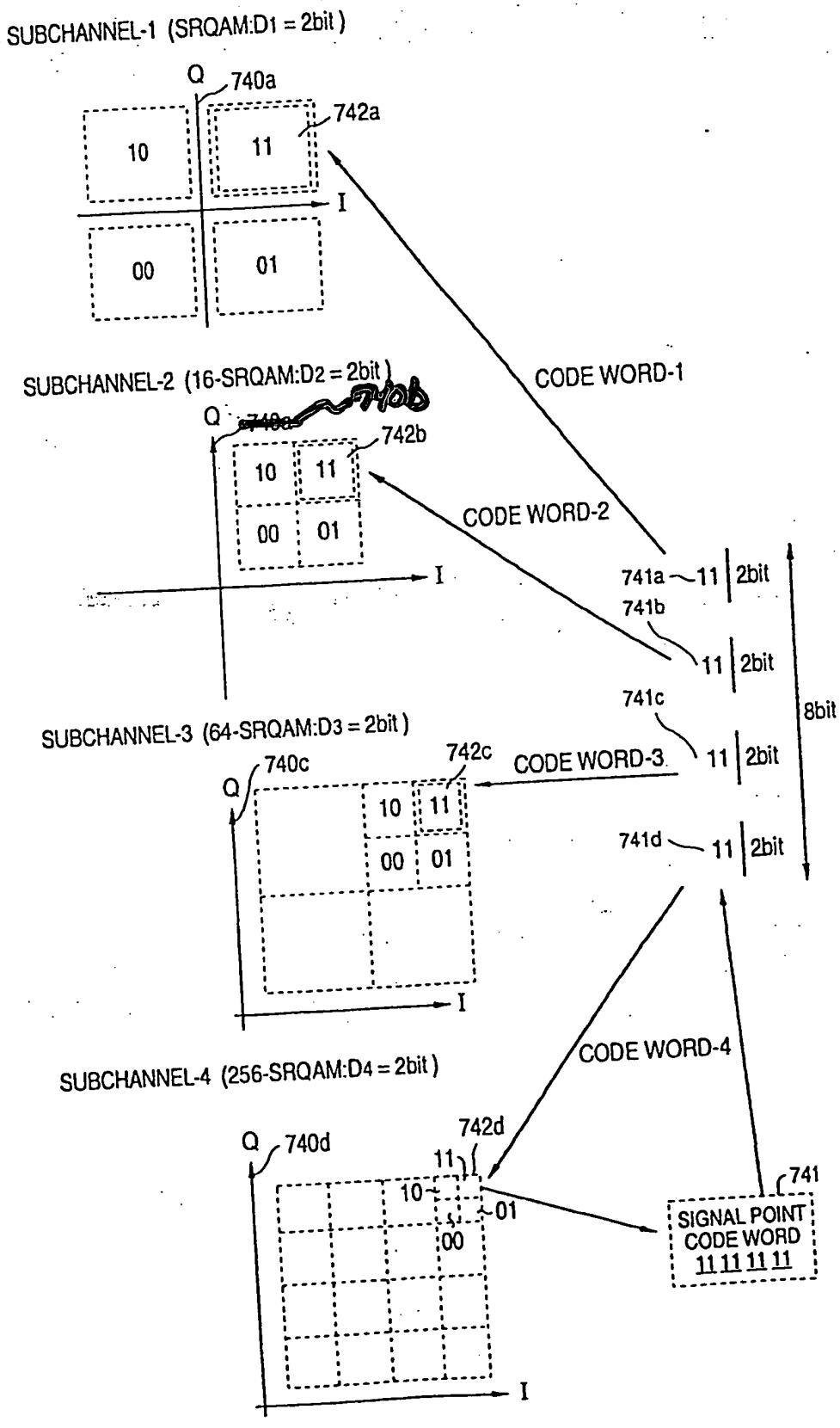

3
DIVIDER
895
772a
MIXER
772b
MIXER
772c
MIXER
404a
DIVIDER
404b
DIVIDER
404c
DIVIDER
HHVH
HLVH
HHVL
HLVL
in
HHVH-HLVL
405d
COMPRESSOR
405c
COMPRESSOR
405b
COMPRESSOR
405a
COMPRESSOR
HH
HL
LH
LL
D2-2
D2-1
D1-2
D1-1

FIG. 93

FIG. 112


SUBCHANNEL-1 (SRQAM:D1 = 2bit)
Q
740a
742a
10
11
I
00
01
CODE WORD-1
SUBCHANNEL-2 (16-SRQAM:D2 = 2bit)
740b
Q
742b
10
11
00
01
I
CODE WORD-2
741a
11
2bit
741b
11
2bit
741c
11
2bit
8bit
SUBCHANNEL-3 (64-SRQAM:D3 = 2bit)
740c
742c
CODE WORD-3
Q
10
11
00
01
I
741d
11
2bit
CODE WORD-4
SUBCHANNEL-4 (256-SRQAM:D4 = 2bit)
Q
740d
742d
11
10
01
00
I
741
SIGNAL POINT
CODE WORD
11 11 11 11

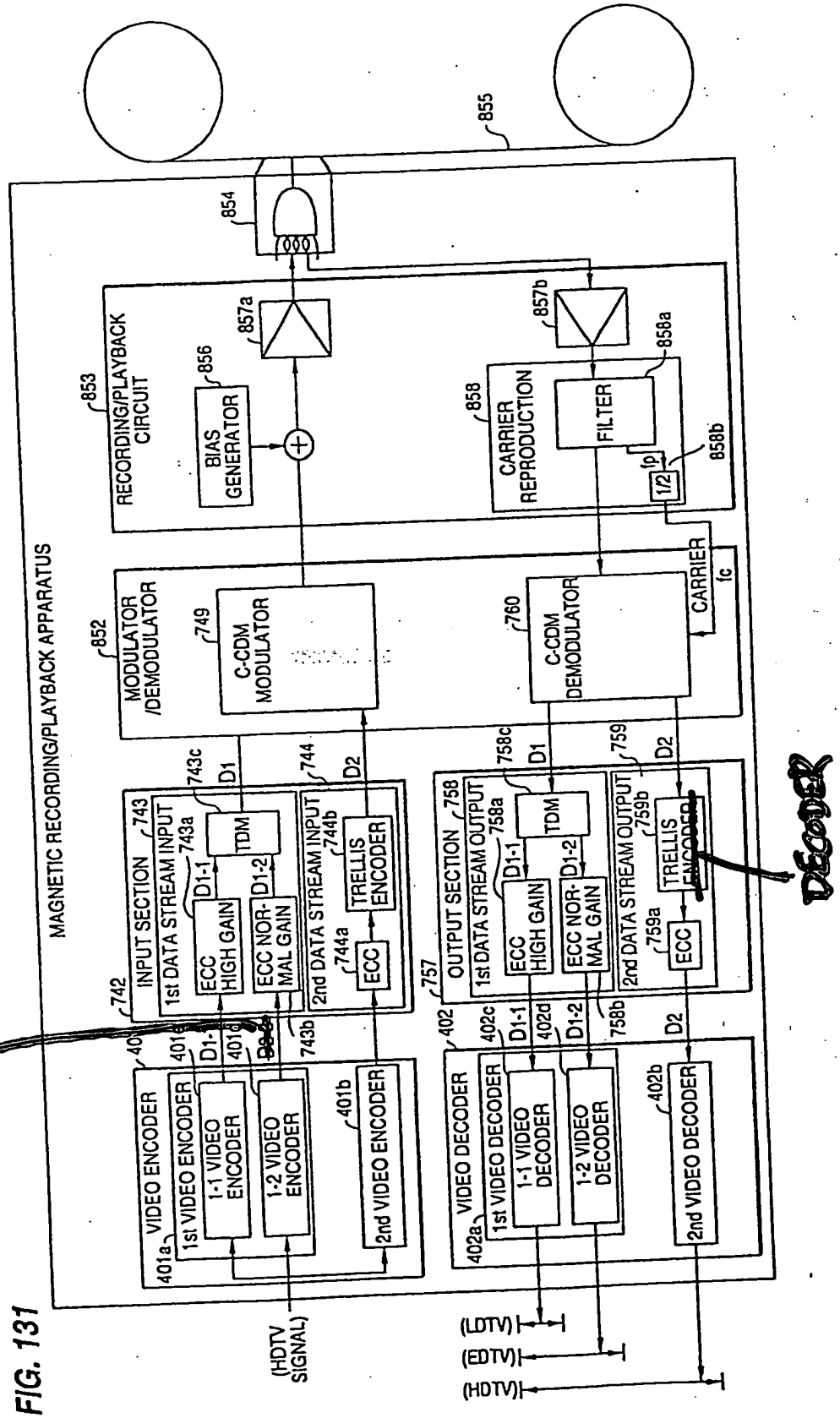

MAGNETIC RECORDING/PLAYBACK APPARATUS
855
854
RECORDING/PLAYBACK CIRCUIT
853
BIAS GENERATOR
856
857a
857b
CARRIER REPRODUCTION
858
FILTER
858a
858b
1/2
1p
MODULATOR /DEMODULATOR
852
C-CDM MODULATOR
749
C-CDM DEMODULATOR
760
CARRIER
fc
INPUT SECTION
743
1st DATA STREAM INPUT
743a
2nd DATA STREAM INPUT
744b
744a
ECC
HIGH GAIN
ECC NOR-MAL GAIN
TDM
TRELLIS ENCODER
D1-1
D1-2
D1
D2
743c
744
743b
742
OUTPUT SECTION
758
1st DATA STREAM OUTPUT
758a
2nd DATA STREAM OUTPUT
759b
759a
758c
759
758b
757
VIDEO ENCODER
401a
1st VIDEO ENCODER
1-1 VIDEO ENCODER
1-2 VIDEO ENCODER
2nd VIDEO ENCODER
401b
VIDEO DECODER
402a
1st VIDEO DECODER
1-1 VIDEO DECODER
1-2 VIDEO DECODER
2nd VIDEO DECODER
402b
402c
402d
(HDTV SIGNAL)
(LDTV)
(EDTV)
(HDTV)
D-a
DECODER

FIG. 131

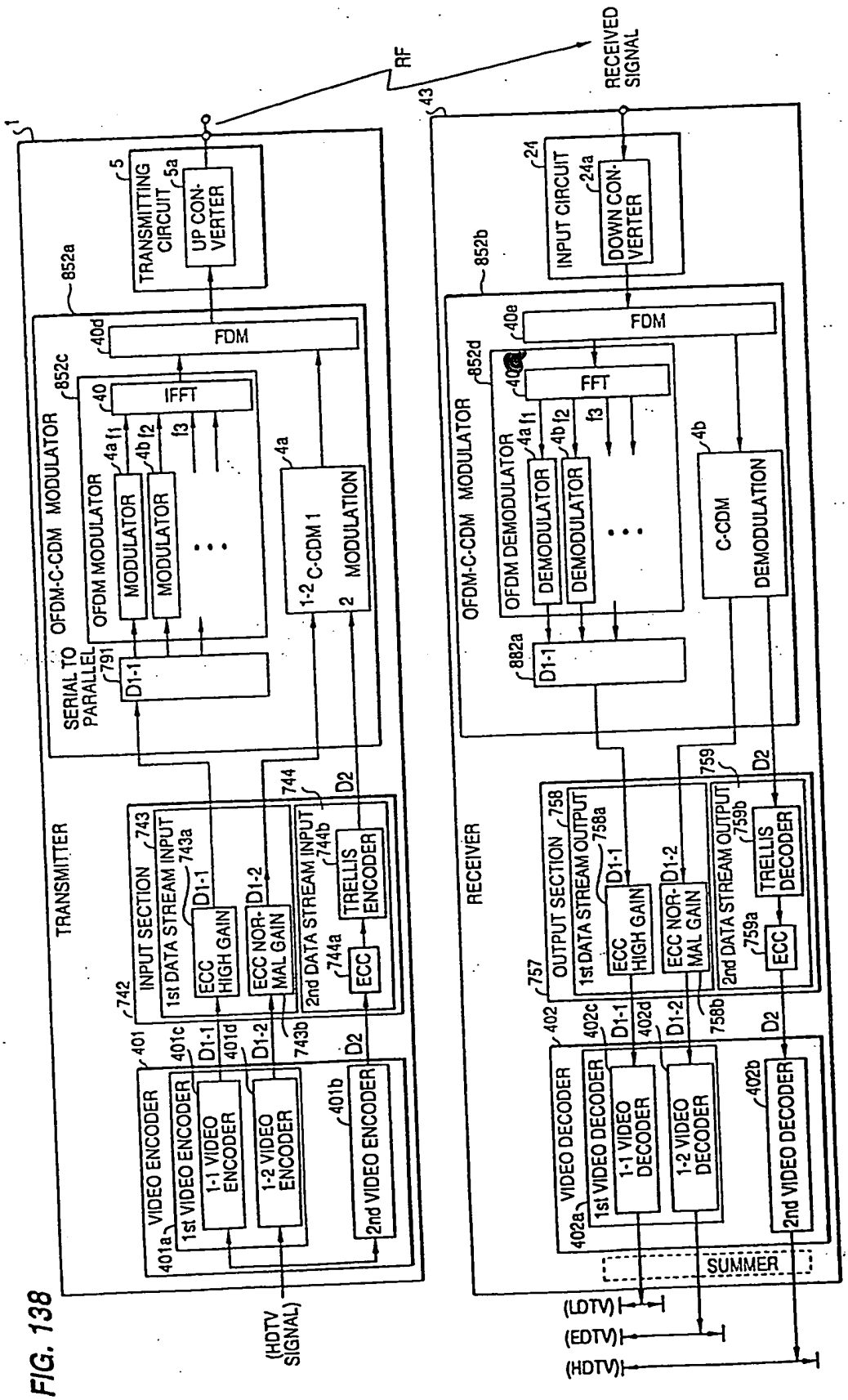

TRANSMITTER
RECEIVER
RF
RECEIVED SIGNAL
(HDTV SIGNAL)
TRANSMITTING CIRCUIT
UP CONVERTER
INPUT CIRCUIT
DOWN CONVERTER
OFDM-C-CDM MODULATOR
OFDM-C-CDM DEMODULATOR
SERIAL TO PARALLEL
OFDM MODULATOR
OFDM DEMODULATOR
MODULATOR
DEMODULATOR
FDM
FFT
1-2 C-CDM
MODULATION
C-CDM
DEMODULATION
INPUT SECTION
OUTPUT SECTION
1st DATA STREAM INPUT
2nd DATA STREAM INPUT
1st DATA STREAM OUTPUT
2nd DATA STREAM OUTPUT
ECC
HIGH GAIN
ECC NORMAL GAIN
TRELLIS ENCODER
TRELLIS DECODER
VIDEO ENCODER
1st VIDEO ENCODER
1-1 VIDEO ENCODER
1-2 VIDEO ENCODER
2nd VIDEO ENCODER
VIDEO DECODER
1st VIDEO DECODER
1-1 VIDEO DECODER
1-2 VIDEO DECODER
2nd VIDEO DECODER
SUMMER
(SDTV)
(EDTV)
(HDTV)

FIG. 138

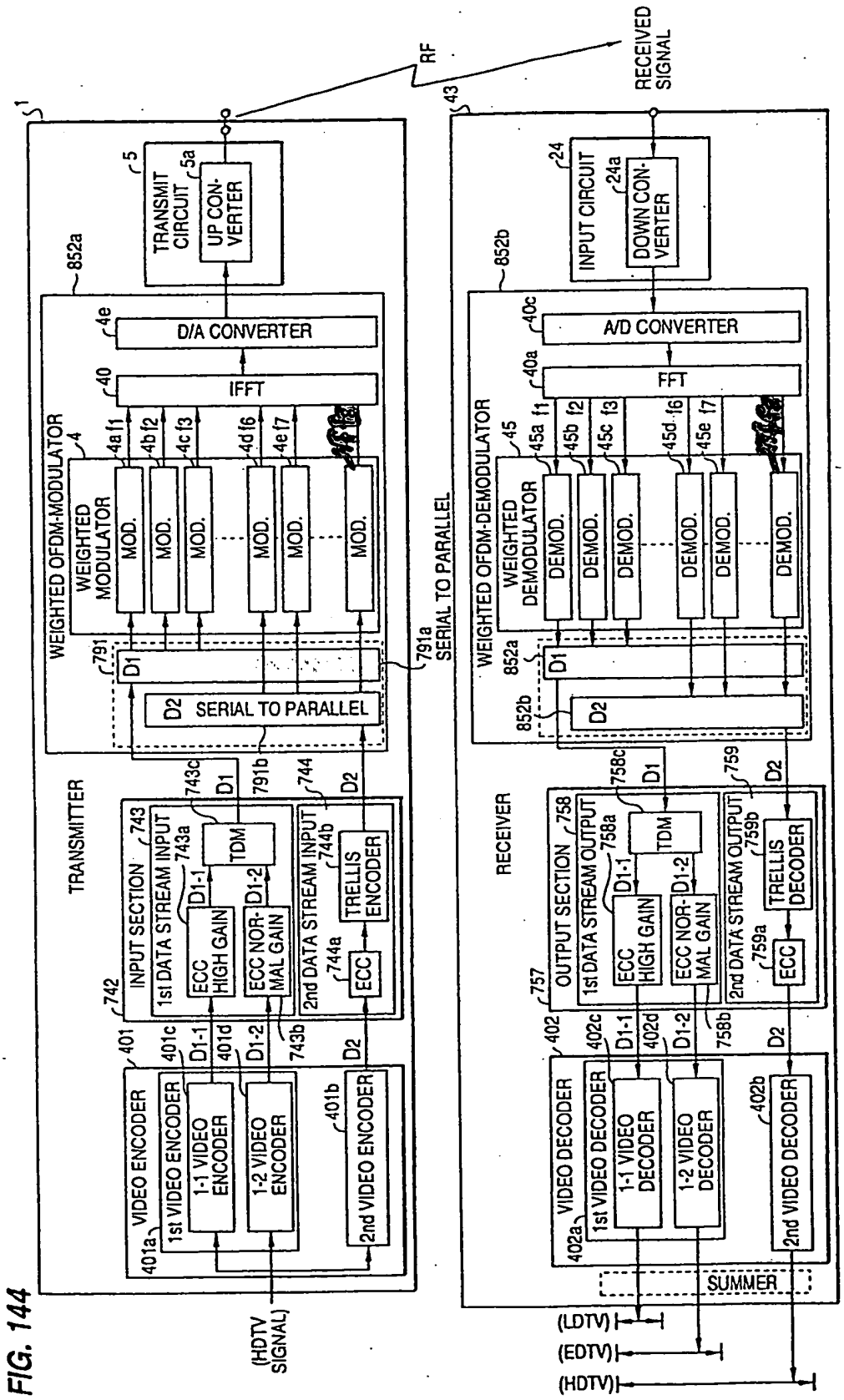
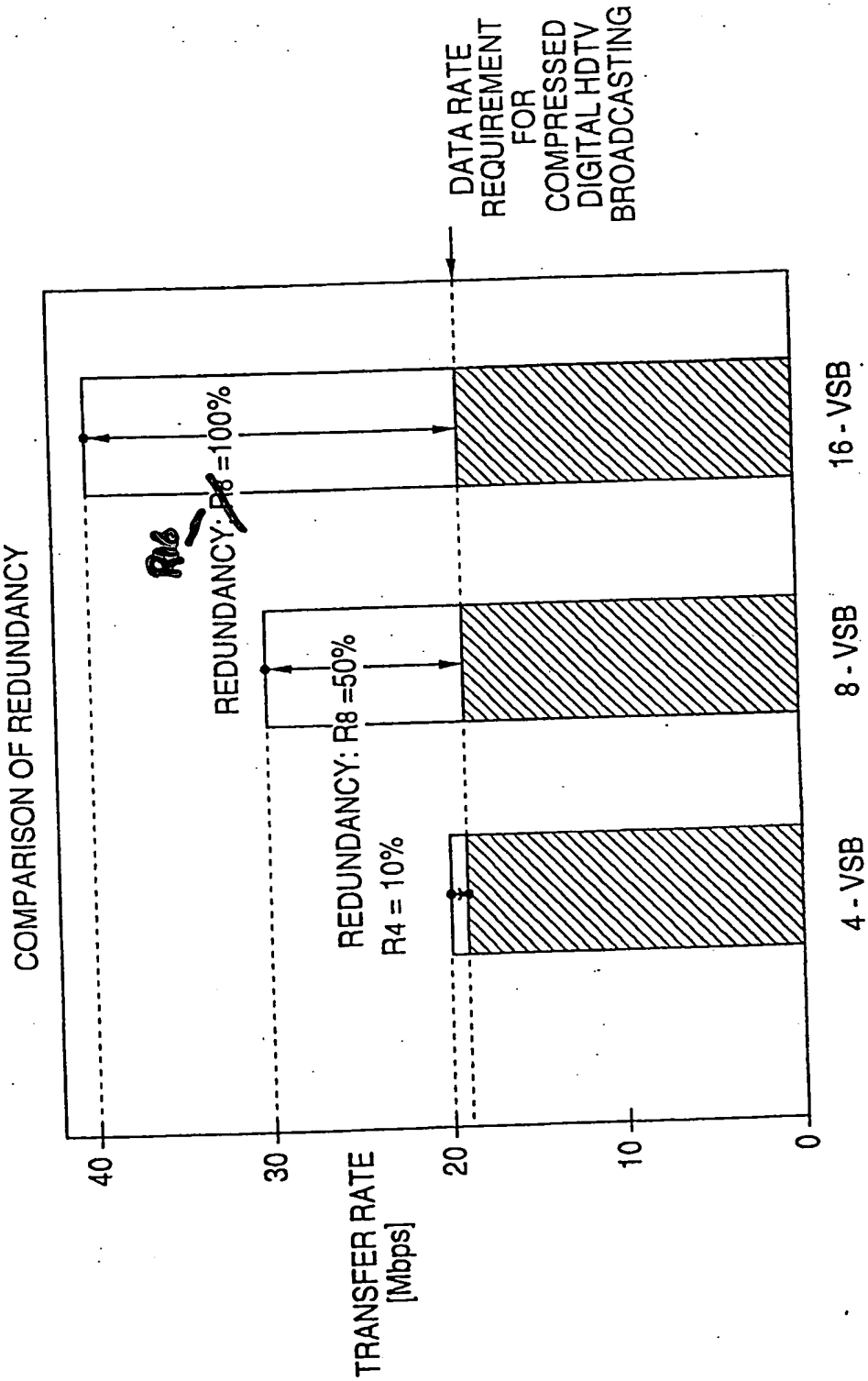

TRANSMITTER
RECEIVER
RF
RECEIVED SIGNAL
TRANSMIT CIRCUIT
UP CONVERTER
INPUT CIRCUIT
DOWN CONVERTER
D/A CONVERTER
A/D CONVERTER
IFFT
FFT
WEIGHTED OFDM-MODULATOR
WEIGHTED OFDM-DEMODULATOR
WEIGHTED MODULATOR
WEIGHTED DEMODULATOR
MOD.
DEMOD.
SERIAL TO PARALLEL
INPUT SECTION
1st DATA STREAM INPUT
2nd DATA STREAM INPUT
ECC HIGH GAIN
ECC NORMAL GAIN
TRELLIS ENCODER
TDM
OUTPUT SECTION
1st DATA STREAM OUTPUT
2nd DATA STREAM OUTPUT
TRELLIS DECODER
VIDEO ENCODER
1st VIDEO ENCODER
1-1 VIDEO ENCODER
1-2 VIDEO ENCODER
2nd VIDEO ENCODER
VIDEO DECODER
1st VIDEO DECODER
1-1 VIDEO DECODER
1-2 VIDEO DECODER
2nd VIDEO DECODER
SUMMER
(HDTV SIGNAL)
(LDTV)
(EDTV)
(HDTV)

FIG. 144

FIG. 169


COMPARISON OF REDUNDANCY
DATA RATE REQUIREMENT FOR COMPRESSED DIGITAL HDTV BROADCASTING
REDUNDANCY: R8 =100%
REDUNDANCY: R8 =50%
REDUNDANCY: R4 = 10%
16 - VSB
8 - VSB
4 - VSB
TRANSFER RATE [Mbps]
40
30
20
10
0